IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please amend claims 1-10, 13, and 16-18 as follows:

1. (**CURRENTLY AMENDED**) An apparatus generating ~~an~~ error flags for a data frame including a plurality of ECC (Error-Correction Coding) data blocks, wherein each ECC data block is located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error, the apparatus comprising:

a frame-sync error memory which stores frame-sync error information for at least one of the ECC data blocks;

a BIS ~~(Burst Indicator Subcode)~~ error flag memory which stores a BIS error flag for the at least one ECC data block; and

an error flag generator, which generates one of the~~an~~ error flags indicating an error existence/absence for a corresponding one of the ECC ~~(Error-Correction Coding)~~ data blocks with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

2. (**CURRENTLY AMENDED**) The apparatus of claim 1, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two of the ECC data blocks.

3. (**CURRENTLY AMENDED**) The apparatus of claim 1, wherein the at least one ECC data block has an error correction format in which the frame-sync data is recorded in a heading of the at least one ECC data block and BIS data columns are recorded between sets of ECC data columns, and

the error flag generator generates an error flag indicating an error existence for an entire ECC data constructing a set of ECC data columns with reference to error information stored in

the frame-sync error memory and the BIS error flag memory, if both the frame-sync error information of the frame-sync data and the BIS error flag of one of the BIS data columns neighboring thea set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring the set ~~a pair~~ of the ECC data columns, indicate the error existence.

4. (**CURRENTLY AMENDED**) The apparatus of claim 1, further comprising a frame-sync detector, which receives a reproduced digital signal for the at least one ECC data block, determines the error existence/absence for frame-sync data for the at least one ECC data block, and outputs frame-sync error information to the frame-sync error memory.

5. (**CURRENTLY AMENDED**) An error flag generation method comprising:

receiving a reproduced digital signal;

generating frame-sync error information for at least one Error Correction Coding (ECC) data block located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error, using the reproduced digital signal;

storing the frame-sync error information in a frame-sync error memory for the at least one ECC data block;

generating a BIS error flag for the at least one ECC data block;

storing the BIS error flag in a BIS error flag memory for the at least one ECC data block; and

generating ~~an~~ error flags indicating error existence/absence for a corresponding ECC data block with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

6. (**CURRENTLY AMENDED**) The method of claim 5, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two ECC data blocks.

7. (**CURRENTLY AMENDED**) The method of claim 5, wherein the at least one ECC data block has an error correction format in which the frame-sync data is recorded in a heading of the at least one ECC data block and BIS data columns are recorded respectively between sets of ECC data columns, and the generating of the error flag comprises generating an error flag

indicating the error existence for an entire ECC data constructing a set of ECC data columns, with reference to error information stored in the frame-sync error memory and the BIS error flag memory, if both the frame-sync error information of the frame-sync data and the BIS error flag of a BIS data column neighboring the set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring the set of the ECC data columns, indicate error existence.

8. (**CURRENTLY AMENDED**) An apparatus generating ~~an~~ error flags for a data frame including a plurality of ECC (Error-Correction Coding) data blocks, wherein each ECC data block is located between frame-sync data and BIS (Burst Indicator Subcode) data or between two of the BIS data, the BIS data comprising information that is inserted in order to indicate a generation of a burst error, comprising:

a frame-sync detector, outputting frame-sync error information indicating an existence/absence of an error for frame sync-data of frames forming the ECC data blocks;

a frame-sync error memory, storing the frame-sync error information of the frames forming the ECC data blocks;

a BIS (Burst Indicator Subcode) error flag memory, storing a BIS error flag for the ECC data blocks; and

an error flag generator, generating one of the~~an~~ error flags indicating an existence/absence of an error for a corresponding one of the ECC ~~(Error-Correction Coding)~~ data blocks with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

9. (**CURRENTLY AMENDED**) The apparatus of claim 8, wherein the frame-sync error memory stores frame-sync error information corresponding to at least two of the ECC data blocks.

10. (**CURRENTLY AMENDED**) The apparatus of claim 8, wherein the BIS error flag memory stores BIS error flags corresponding to at least two of the ECC data blocks.

11. (**ORIGINAL**) The apparatus of claim 8, wherein the frame-sync error memory comprises a first through N-th frame-sync error memories.

12. (**ORIGINAL**) The apparatus of claim 11, wherein N is at least two.

13. (**CURRENTLY AMENDED**) The apparatus of claim 11, wherein each of the frame-sync error memories has a size of 1x496 bits, and stores frame-sync error information of at least one of the ECC data blocks.

14. (**ORIGINAL**) The apparatus of claim 8, wherein the BIS error flag memory comprises a first through an M-th BIS error memories.

15. (**ORIGINAL**) The apparatus of claim 14, wherein M is at least two.

16. (**CURRENTLY AMENDED**) The apparatus of claim 14, wherein each of the BIS error memories has a size of 1x496 bits, and stores a BIS error flag of at least one of the ECC data blocks.

17. (**CURRENTLY AMENDED**) The apparatus of claim 8, wherein each of the ECC data blocks has an error correction format in which frame-sync data is recorded in a heading of the ECC data block and BIS data columns are recorded between sets of ECC data columns.

18. (**CURRENTLY AMENDED**) The apparatus of claim 17, wherein the error flag generator~~,~~ generates an error flag indicating the existence of an error for an entire ECC data forming one of the~~a~~ sets of ECC data columns with reference to error information stored in the frame-sync error memory and the BIS error flag memory, if the frame-sync error information of the frame-sync data and the BIS error flag of the BIS data column neighboring the~~a~~ set of the ECC data columns, or the BIS error flag of the BIS data columns neighboring the~~a~~ set of the ECC data columns, indicate error existence.